

# **Exhibit 19**

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FAIRCHILD SEMICONDUCTOR CORP.

10 UNITED STATES DISTRICT COURT  
11 FOR THE NORTHERN DISTRICT OF CALIFORNIA  
12 SAN FRANCISCO DIVISION  
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14 ALPHA & OMEGA SEMICONDUCTOR,  
15 INC., a California corporation; and  
16 ALPHA & OMEGA SEMICONDUCTOR,  
LTD., a Bermuda corporation,

17 Plaintiffs and Counterdefendants,

18 v.

19 FAIRCHILD SEMICONDUCTOR  
CORP., a Delaware corporation,

20 Defendant and Counterclaimant.

21  
22 AND RELATED COUNTERCLAIMS.  
23

Case No. C 07-2638 JSW  
(Consolidated with Case No. C 07-2664 JSW)

**FAIRCHILD SEMICONDUCTOR  
CORPORATION'S AMENDED  
DISCLOSURE OF ASSERTED CLAIMS  
AND PRELIMINARY INFRINGEMENT  
CONTENTIONS**

**(Patent L.R. 3-1)**

24 Pursuant to Northern District of California Patent Local Rule 3-1, defendant and  
25 counterclaimant Fairchild Semiconductor Corporation ("Fairchild") hereby serves its Amended  
26 Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Disclosure") for U.S.  
27 Patent Nos. 6,429,481, 6,521,497, 6,710,406, and 6,828,195. This Disclosure is based on information  
28 reasonably available to Fairchild at this time. Fairchild reserves the right to supplement this

1 Disclosure based on information developed in the course of this lawsuit through discovery or  
 2 additional factual investigation, in view of the Court's claim construction ruling or as other  
 3 circumstances may require.

#### 4 **I. ASSERTED CLAIMS AND ACCUSED PRODUCTS**

5 Based upon the information presently available, Fairchild contends that plaintiffs and  
 6 counterdefendants Alpha & Omega Semiconductor, Inc., and Alpha & Omega Semiconductor, Ltd.,  
 7 (collectively, "AOS") have infringed and continue to infringe, directly and/or indirectly, the following  
 8 claims of U.S. Patent Nos. 6,429,481 ("the '481 patent"), 6,521,497 ("the '497 patent"), 6,710,406  
 9 ("the '406 patent") and 6,828,195 ("the '195 patent") (collectively, "the Fairchild patents-in-suit") by  
 10 making, using, offering to sell, selling within the United States, or importing into the United States the  
 11 following accused products of which Fairchild is presently aware (or importing into the United States  
 12 products made by methods claimed in the Fairchild patents-in-suit).

14 Patent Number	Asserted Claims	Accused Products
15 The '481 patent	16 Claims 1-4, 6-8, 10, 11, 18, 21 (against accused products with closed cell design) 17 Claims 1-4, 6-11, 15-18, 21, 22 (against accused products with striped design)	See attached Exhibit 1
18 The '497 patent	19 Claims 1-7, 8, 9, 11-13, 15-17 (against accused products with closed cell design) 20 Claims 1-9, 11-13, 15-17 (against accused products with striped design)	See attached Exhibit 1
21 The '406 patent	22 Claims 1-6, 10-12, 13-15, 17, 23 25-32 (against accused products with closed cell design) 24 Claims 1-6, 10-17, 24-32 (against accused products with striped design)	See attached Exhibit 1
25 The '195 patent	26 Claims 1, 2, 6-13, 15-17, 21, 22 (against accused products with closed cell design) 27 Claims 1, 2, 6-13, 15-22 (against accused products with striped design)	See attached Exhibit 1

## **II. CLAIM CHARTS**

Claim charts identifying specifically where each element of each asserted claim is found within each accused device or the process by which each accused device was made are attached hereto as Exhibits 2 through 57. These claim charts are based on information available to Fairchild at this time and are based, in part, upon reverse engineering of a reasonable sampling of AOS products. Fairchild contends that each of the accused AOS products meets the limitations of the asserted claims because, based upon their published characteristics, they are likely to have the same design and structure as the products for which reverse engineering data is provided. In addition, each of the accused AOS products is likely to have been manufactured using a process that is the same or similar in all respects relevant to the asserted claims as the products for which reverse engineering data is provided.

To date, AOS has not provided all of the requested discovery. Additionally, prior to the commencement of this litigation, on May 17, 2007, Fairchild requested that AOS produce, subject to a confidentiality agreement, information regarding the processes by which the accused products are manufactured. AOS refused to produce the information. Consequently, Fairchild is likely to have additional evidentiary support regarding AOS's infringement after a reasonable opportunity for further investigation and discovery.

## **III. INFRINGEMENT**

Fairchild contends that, when the terms of the asserted claims are properly construed, each limitation of each asserted claim is literally present in the corresponding accused device or in the process used to manufacture the accused device as set forth in Sections II above. In the alternative, if warranted by the Court's claim construction, Fairchild reserves the right to contend that any element not found to be literally present in an accused product is present under the doctrine of equivalents.

## **IV. PRIORITY DATES**

Fairchild contends that the asserted claims for each of the Fairchild patents-in-suit are entitled to a priority date of November 14, 1997.

## **V. FAIRCHILD'S PRACTICE OF THE CLAIMED INVENTIONS**

Fairchild wishes to preserve the right to rely, for any purpose, on the assertion that its own

1 products and/or processes practice the inventions claimed in each of the asserted claims. Accordingly,  
 2 Fairchild identifies the following products and/or processes that incorporate or reflect the limitations  
 3 of the corresponding asserted claims.

4 Patent Number	Asserted Claims	Fairchild's Products and/or Processes
5 6,429,481	1, 2, 3, 4, 6, 7, 8, 9, 6 10, 11, 15, 16, 17, 18, 7 21, 22	PowerTrench® MOSFETs
8 6,521,497		None
9 6,710,406	1, 2, 3, 4, 5, 6, 10, 11, 10 12, 13, 14, 15, 16, 17, 11 24, 25, 26, 27, 29, 30, 12 31, 32	PowerTrench® MOSFETs
13 6,828,195	1, 2, 6, 7, 13, 15, 16, 14 17, 18, 19, 20, 21, 22	PowerTrench® MOSFETs

#### 15 VI. PRODUCTION OF DOCUMENTS

16 Fairchild previously produced documents within its possession, custody, or control required by  
 17 Northern District of California Patent Local Rule 3-2.

18 ////

1 DATED: February 25, 2008

Respectfully submitted,

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4 By 

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**CERTIFICATE OF SERVICE**

[C.C.P. §§ 1011 and 1013, C.R.C. § 2008, F.R.C.P. Rule 5, F.R.A.P. 25]

I declare that I am employed in the City and County of San Francisco, California; I am over the age of 18 years and not a party to the within action; my business address is Two Embarcadero Center, Eighth Floor, San Francisco, California, 94111. On the date set forth below, I served a true and accurate copy of the document(s) entitled:

**FAIRCHILD SEMICONDUCTOR CORPORATION'S AMENDED  
DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY  
INFRINGEMENT CONTENTIONS**

on the party(ies) in this action by placing said copy(ies) in a sealed envelope each addressed as follows:

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☐ [By First Class Mail] I am readily familiar with my employer's practice for collecting and processing documents for mailing with the United States Postal Service. On the date listed herein, following ordinary business practice, I served the within document(s) at my place of business, by placing a true copy thereof, enclosed in a sealed envelope, with postage thereon fully prepaid, for collection and mailing with the United States Postal Service where it would be deposited with the United States Postal Service that same day in the ordinary course of business.

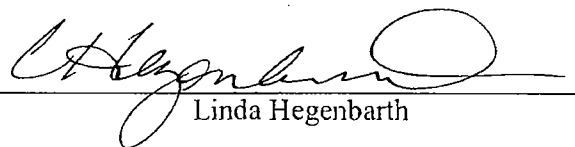
☐ [By Overnight Courier] I caused each envelope to be delivered by a commercial carrier service for overnight delivery to the offices of the addressee(s).

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☐ [By Electronic Transmission] I caused said document to be sent by electronic transmission to the e-mail address(es) indicated for the party(ies) listed above.

I declare under penalty of perjury that the foregoing is true and correct and that this declaration was executed February 25, 2008 at San Francisco, California.

  
Linda Hegenbarth

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# **Exhibit 1**



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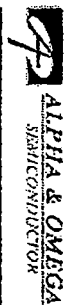
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## MOSFET Selector Guide - All Products

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## MOSFET Selector Guide - All Products

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## MOSFET Selector Guide - All Products

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**AMENDED EXHIBIT 6****INFRINGEMENT OF U.S. PATENT NO. 6,429,481****AOS AO4410 POWER MOSFET**

<b>CLAIM</b>	<b>AO4410 POWER MOSFET</b>
1. A trench field effect transistor comprising:	The AOS AO4410 Power MOSFET ("the accused device") is a trench field effect transistor. (Fig. AO4410-1 (datasheet); Fig. AO4410-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4410-1 (datasheet); Fig. AO4410-3 (Scanning Electron Microscopy image), item A; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4410-3 (Scanning Electron Microscopy image), item C; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

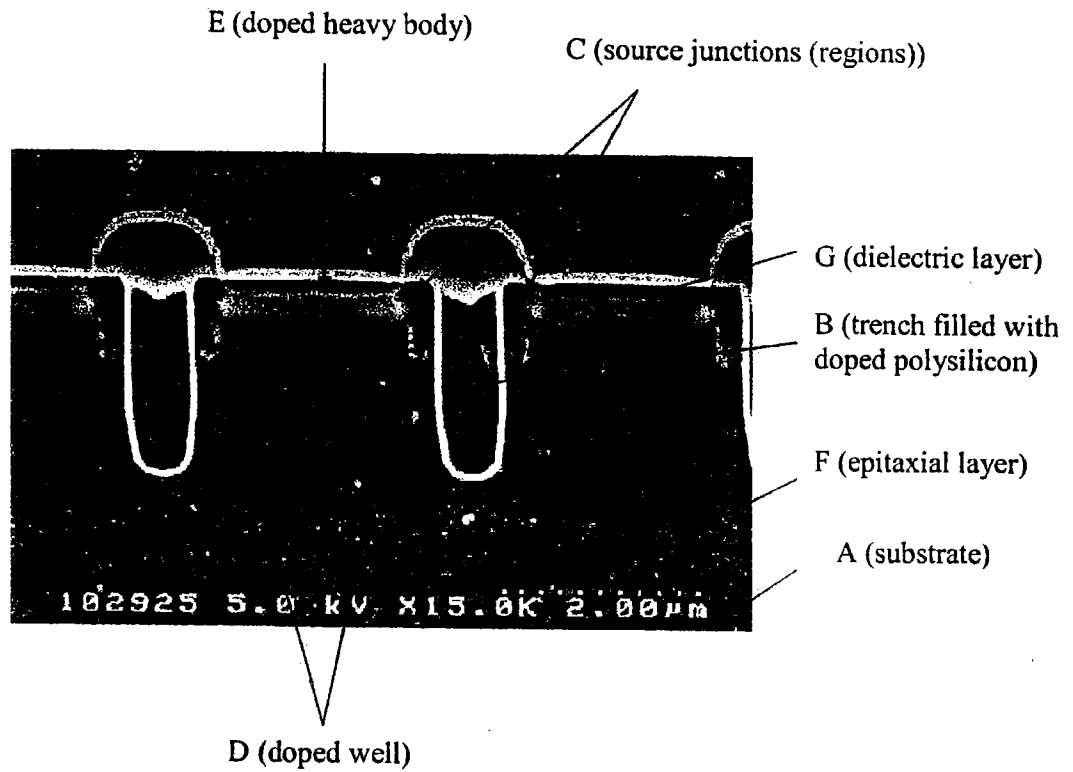
CLAIM	AO4410 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
6. An array of transistor cells comprising:	The accused device has an array of transistor cells. (Fig. AO4410-7 (Scanning Electron Microscopy image), item H.)
a semiconductor substrate having a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4410-1 (datasheet); Fig. AO4410-3 (Scanning Electron Microscopy image), item A; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;	The accused device has gates formed using a design with substantially parallel trenches, with the trenches extending to a predetermined depth into the substrate and contact areas formed between the parallel trenches. (Fig. AO4410-7 (Scanning Electron Microscopy image), items I and L; Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench and extending along the length of the trench. (Fig. AO4410-3 (Scanning Electron Microscopy image), item C; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate between each pair of gate-forming trenches. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is formed inside the doped well and positioned adjacent to each source junction. The deepest portion of the P-type heavy body extends to a depth in the substrate that is less than the predetermined depth of the trenches. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)
alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,	The accused device has alternating doped heavy body and source contact regions at the surface of the substrate along the length of the contact area. (Fig. AO4410-7, items J and K.)



CLAIM	AO4410 POWER MOSFET
wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.	The junction between the highly doped P-type heavy body and the lightly doped P-type well is an abrupt junction. This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
7. The array of transistor cells of claim 6, wherein each said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
8. The array of transistor cells of claim 6 wherein the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.	The depth of the abrupt junction is selected to cause the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
10. The array of transistor cells of claim 6 wherein each said gate-forming trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
11. The array of transistor cells of claim 9 further comprising a field termination structure surrounding the periphery of the array.	The accused device has a field termination structure surrounding the periphery of the array. (Fig. AO4410-6, item A.)
18. The trench field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4410-3 (Scanning Electron Microscopy image), item F; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.
21. The trench field effect transistor of claim 6, further comprising:	
an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4410-3, item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

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**FIGURE AO4410-3**



**FIGURE AO4410-4**

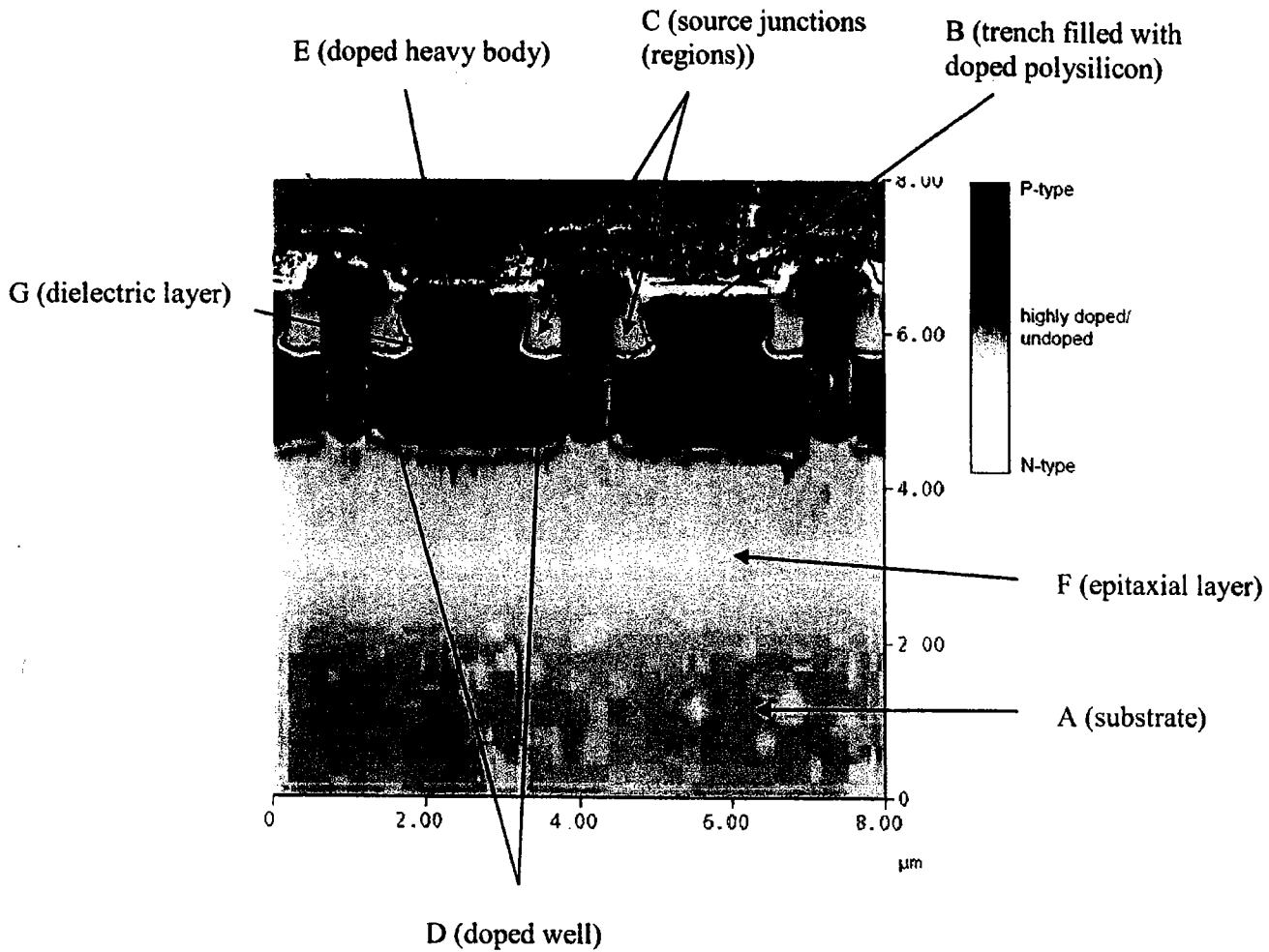
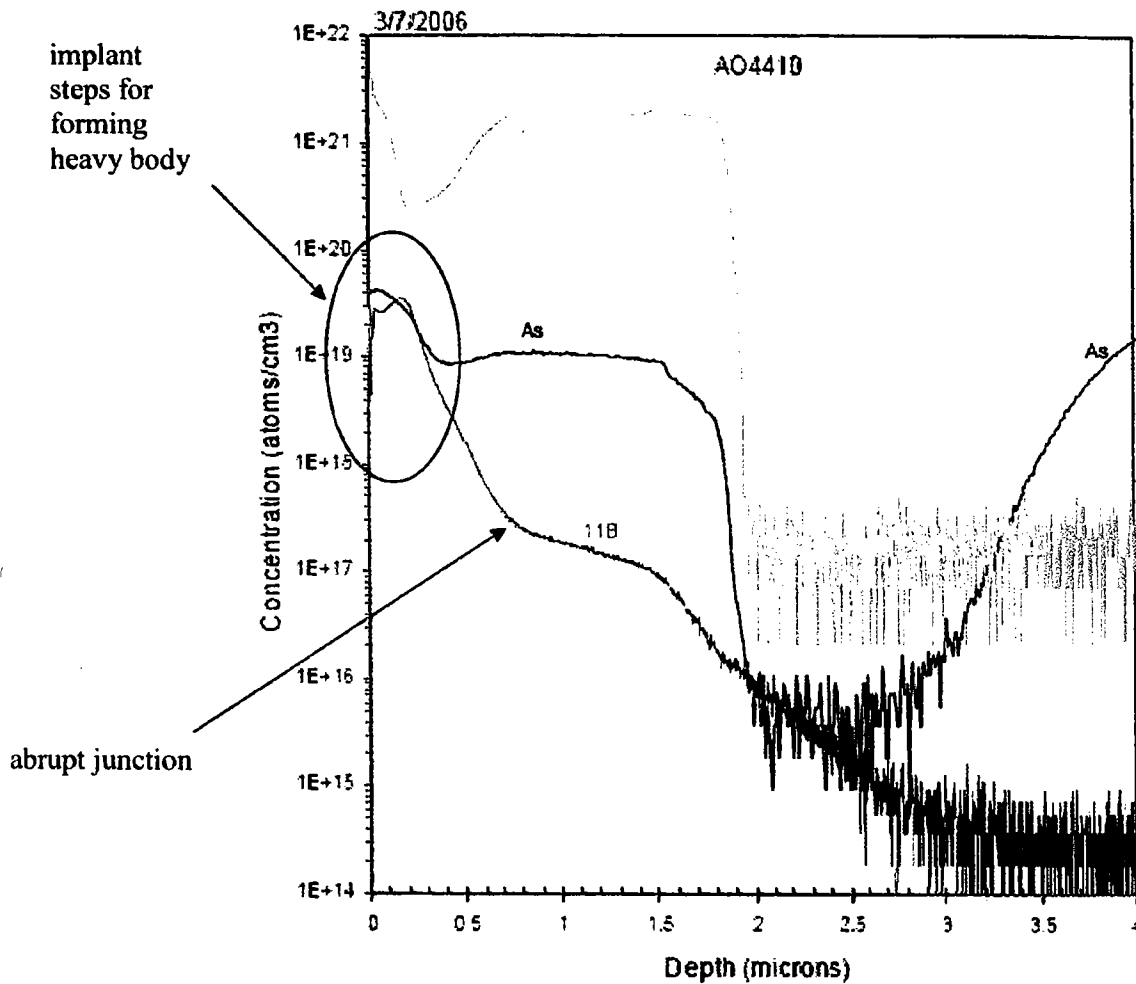


FIGURE AO4410-5



Secondary Ion Mass Spectroscopy Data for Boron, Arsenic, and Oxygen in MOSFET Array for AO4410